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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/665,713 | 09/19/2003 | Douglas Duane Coolbaugh | BUR920000142US2(13891A) | 6003 |

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| EXAMINER | |
|---|---|
| SEFER, AHMED N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/665,713 | DUPUIS ET AL | |
| | Examiner | Art Unit | |
| | A. Sefer | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. The amendment filed July 22, 2004 has been entered; no new claims have been introduced.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Taka et al. ("Taka") USPN 5,399,511.

Taka discloses (figs. 4 and 13-16 and col. 8, lines 13-26) a method of reducing the dislocations present in a SiGe heterojunction bipolar transistor, said method comprising the steps of: (a) providing a semiconductor substrate comprising a collector region 52 and isolation regions (44,46,49,50) adjacent said collector region, said semiconductor substrate having an upper surface; (b) recessing a portion F including etching of the isolation regions below an upper surface of said collector region in said semiconductor substrate so as to provide a recessed isolation surface; and (c) forming a SiGe layer 58 on the upper surface of the semiconductor substrate as well as said recessed isolation surface, wherein said recessing controls facet formation at edges of the SiGe layer and the upper surface of the collector.

As for claims 2-4, Taka discloses (col. 6, lines 29-43) isolation regions being trench isolation regions formed by trench filling (as in claim 3) including deposition of SiO2 (as in claim 4).

As for claims 5 and 6, Taka discloses a patterned dielectric layer 49 composed of a nitride (as in claim 6) formed on a portion of said isolation regions prior to conducting step (b).

As for claim 8, Taka discloses a patterned dielectric 50 formed on a portion region that is not recessed.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6, 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Gris USPN 6,352,907 (of record) in view of Sato (JP 2000-269230)

Gris discloses (see figs. 1-9, col. 4, lines 37-54 and col. 5, 10-15) a method of reducing the dislocations present in a SiGe heterojunction bipolar transistor, said method comprising the steps of: (a) providing a semiconductor substrate comprising a collector region 3 and isolation regions 4 adjacent said collector region; (b) recessing a portion 9 including etching of the isolation regions below the upper surface of said semiconductor substrate so as to provide a recessed isolation surface; and (c) forming a SiGe layer 10 on an upper surface of the semiconductor substrate as well as said recessed isolation surface, wherein said recessing

controls facet formation at edges of the SiGe layer and the upper surface of the collector, but does not disclose a recessing portion of the isolation regions below the upper surface of said collector region in said semiconductor substrate.

Sato discloses in figs. 1-12 a method of reducing the dislocations present in a SiGe heterojunction bipolar transistor, said method comprising the steps of: (a) providing a semiconductor substrate comprising a collector region 13 and isolation regions 10/5 adjacent said collector region; (b) recessing a portion 101 of the isolation regions below the upper surface of said collector region in said semiconductor substrate.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Sato's teachings with Gris' invention since that would reduce C-B capacitance as taught by Sato.

As for claims 2-4, Gris discloses (see col. 2, lines 40-53) isolation regions being trench isolation regions formed by trench filling (as in claim 3) including deposition of SiO2 (as in claim 4).

As for claims 5 and 6, Gris discloses a patterned dielectric layer 5-2 composed of a nitride (as in claim 6) formed on a portion of said isolation regions prior to conducting step (b).

As for claim 8, Gris discloses a patterned dielectric 15 formed on a portion region that is not recessed.

As for claim 10, Gris discloses comprising the steps of: (d) forming an insulator 15/11 on said SiGe layer; (e) providing an opening (see fig. 8) in said insulator so as to expose a portion of said SiGe layer; (f) forming an emitter material 12 on said insulator and in said opening so as to

contact said SiGe layer; and (g) patterning said emitter material and said insulator so as to form a patterned emitter and a patterned insulator on said SiGe layer.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gris in view of Sato as applied to claim 1 above and further in view of Kamins et al. ("Kamins") USPN 5,633,179 (of record).

The combined references disclose the method of reducing the dislocations present in a SiGe heterojunction bipolar transistor as recited in the claim, but do not specifically disclose recessing a portion including lithography and etching.

Kamins discloses in figs. 3 and 5 recessing a portion 16/18-22 layers including lithography and etching.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Kamins' since that would provide a proper control of the etch process as taught by Kamins.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gris in view of Sato as applied to claim 1 above and further in view of Heinemann et al. ("Heinemann") (DE 19652423) (of record).

The combined references disclose the method of reducing the dislocations present in a SiGe heterojunction bipolar transistor as recited in the claim, but do not specifically disclose said SiGe layer being formed by a deposition process selected from the group consisting of ultra-high vacuum chemical vapor deposition (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD) and plasma-enhanced chemical vapor (PECVD).

Heinemann et al disclose (see abstract) a SiGe layer being formed by molecular beam epitaxy (MBE).

Therefore, it would have been have obvious to one skilled in the art at the time the invention was made to incorporate Heinemann's since that would reduce the outward diffusion of the SiGe layer as taught by Heinemann.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
September 25, 2004

NATHAN J FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800